ISSN: 2277-9655
Impact Factor: 4.116
CODEN: IJESS7

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

AREA OPTIMIZED ROUTER ARCHITECTURE

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DOI: 10.5281/zenodo.556369

ABSTRACT

This Paper is proposing implementation of Router and verifies the functionality of the three port router with latest verification methodologies. This Router design contains three output ports and one input port, and this design implemented based on packet based Protocol. This proposed router contains Registers and FIFO with error checking. The proposed structure implemented using Verilog hardware description language and on Xilinx 14.7.

KEYWORDS: *Router, FIFO, FSM, Register blocks,* Simulation

INTRODUCTION

Due to functional bugs in ASIC and the functional verification decides the quality of the silicon, and it requires large amount of the design cycle time i.e for the verification/simulation. In order to avoid the delay and meet the time to market, we are going for latest verification methodologies and tools for the verification process.
This project main aim is to understand the functionality of basic router and know about Hardware Verification Languages like Verilog and EDA tools, for the high speed implementation and area optimized design verification.

What is a Router?

It defines a router is not its size, shape, color, or manufacturer, but its job function i. e based on the work it has to doing called routing data packets between computers. A simple cable can't route the data between computers, ISP and different computers a simple modem which routes data between your PC and ISP can be considered a router. In its most basic form, a router could simply be one of two computers running the Windows 98 (or higher) operating system connected together using ICS (Internet Connection Sharing).
Many of the internet users are needed LAN (Local area network) or WLAN (wireless local area network) connection to connect. If the user have more than one computer's it is not possible to connect all the system to single LAN. So, we need an interface to connect many computers to single LAN. This interface is called router.
In many instances, an ISP will allow you to use a router. It is easy to use a single Internet connection for connect multiple computers. It efficient for a simple and smaller home users and pay a nominal internet charge for single internet connection. Without paying extra amount for additional computer's internet sharing. This kind of small router allows you to connect two or more computers with single internet or LAN connection are called broad band routers that enable two or more computers to share an Internet connection. Within a business or organization, you may need to connect multiple computers to the Internet.

DESIGN OF THREE PORT ROUTER

This paper explains specifications for the Router and it is a packet based protocol. Router sends the incoming packet which comes from the input port to output ports based on the address contained in the packet. The router is a "Network Router". It has a one input port from which the packet enters and it has three output ports where the packet is driven out.

Packet format contains three parts. They are Header, data and frame check sequence. Packet width is 8 bits and the length of the packet can be varies between 1 bytes to 63 bytes. Packet header contains three fields DA and length. Destination address (DA) of the packet is of 8 bits. The switch drives the packet to respective ports based

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on this destination address of the packets. Each output port has 8- bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 63. Length is measured in terms of bytes. Data should be in terms of bytes and can take anything. Frame check sequence contains the security check of the packet. It is calculated over the header and data. The communication on network on chip is carried out by means of router, so for implementing better NOC, the router should be efficiently design. This router supports three parallel connections at the same time. It uses store and forward type of flow control and FSM (Finite state machine) Controller deterministic routing which improves the performance of router.

The switching mechanism used here is packet switching which is generally used on network on chip. In packet switching the data transfers in the form of packets between cooperating routers and independent routing decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels. The arbiter is of rotating priority scheme so that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides.

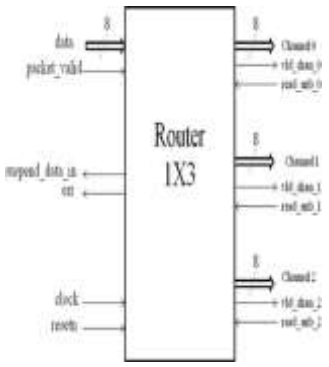

Fig 1 ***Block diagram of three port route***

IMPLEMENTATION&RESULTS

Proposed design can be implemented using Verilog HDL using Xilinx 14.7 software and mount on hardware device Spartan 3. Before this implementation many of network routers are proposed and the bit difference is optimized area compared to existing routers. It is observed by using Device utilization.

Logic Utilization	Used	Available	Utilization
Number of Slices	144	768	18%
Number of Slice Flip Flops	120	1536	7%
Number of 4 input LUTs	273	1536	17%
Number of bonded IOBs	43	124	34%
Number of GCLKs	1	8	12%

Table 1 Device utilization summary

The device utilization summary shown in table-1 and it requires 273 4-input LUTS and 144 slices where as it far less compared to existing technologies. It is clearly shows that it is optimized in area.

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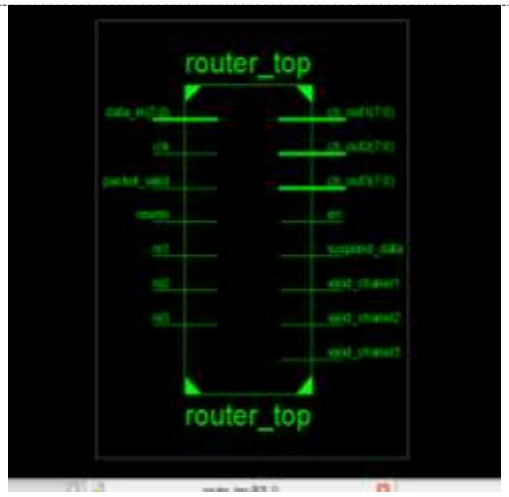

Fig 2 RTL schematic

Fig 2,3,4 shows the RTL schematic, full view of schematic and technology view of optimized router

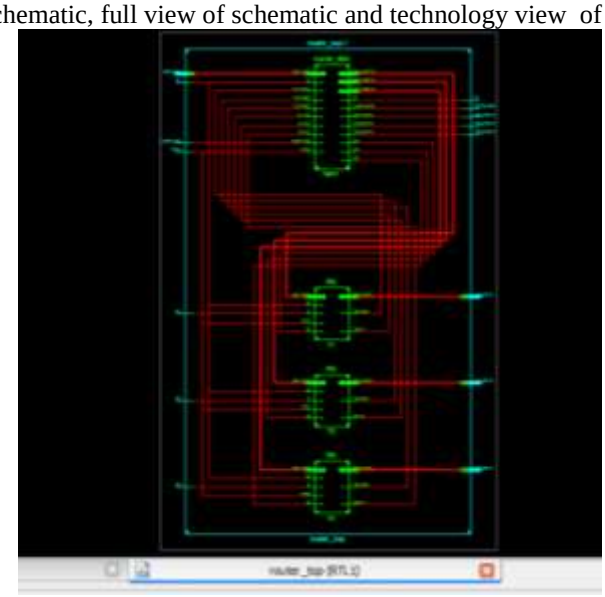

Fig 3 full view of RTL schematic

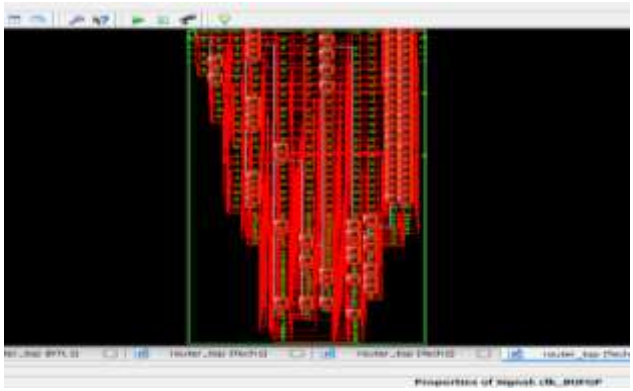

Fig 4 technology view of RTL Schematic

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Fig 5 shows the simulation results of optimized router and it consists of one input port named data_in, three output ports named channel_0, channel_1 and channel_2, data validity bit for packet validation and three read signals are shown in simulation results

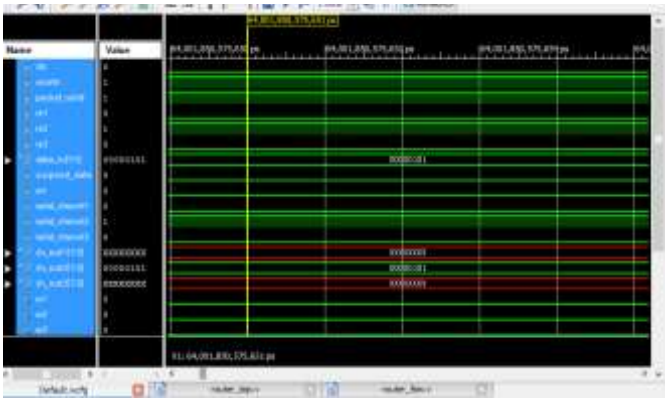

Fig 5 Simulation Result

CONCLUSION

In this OPTIMISED ROUTER implementation observed the functionality of ROUTER with the latest Design methodology i.e., Verilog and System Verilog. In any VLSI architecture the main constraint is area; by using this implementation area is optimized.

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